FIG. 1

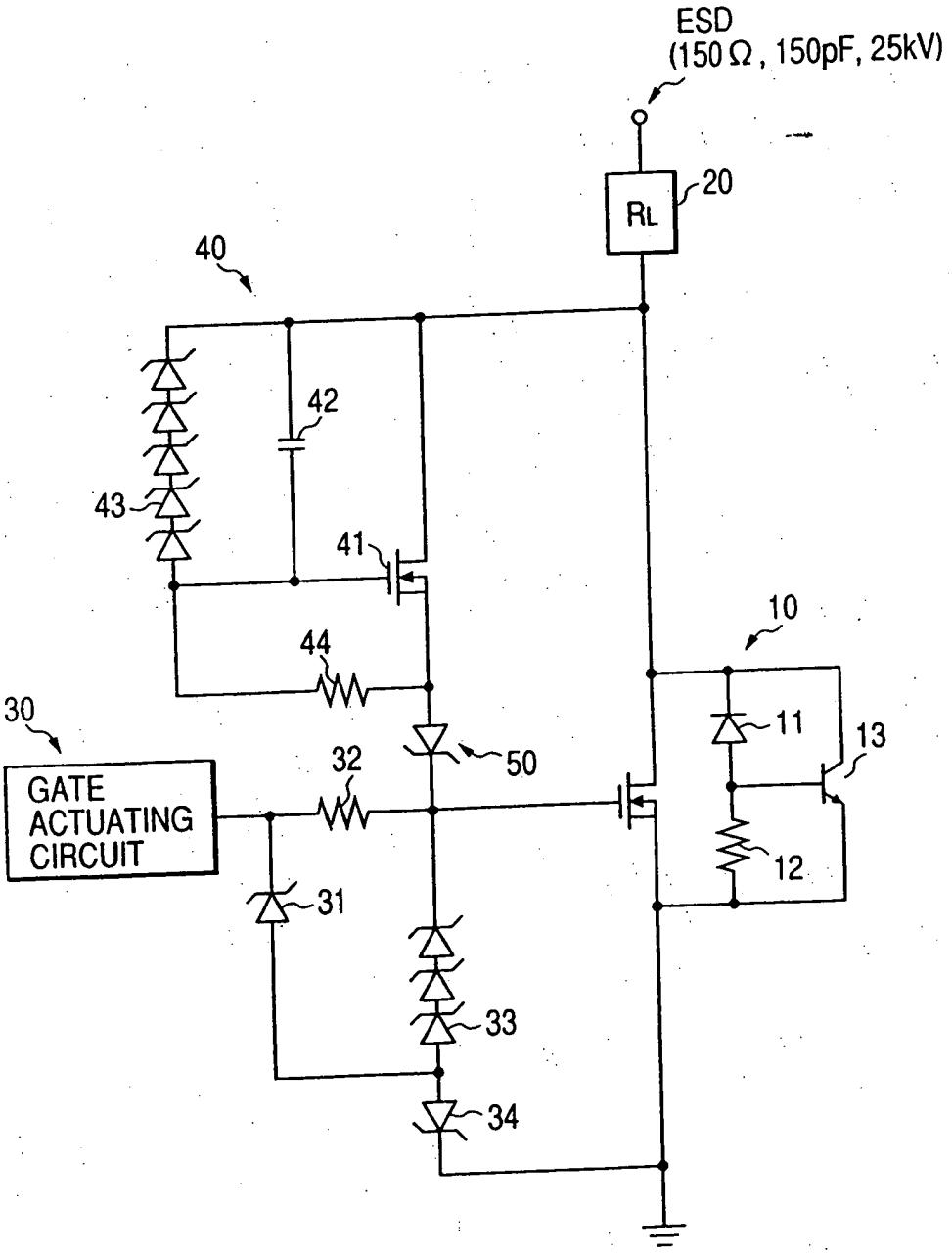


FIG. 2A

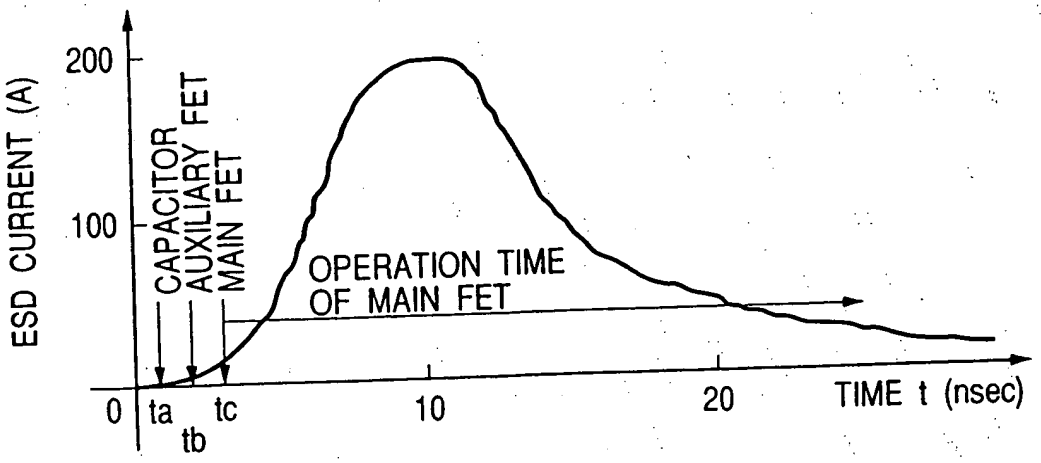

ESD CURRENT (A)
200
100
0
ta
tb
tc
CAPACITOR
AUXILIARY FET
MAIN FET
OPERATION TIME
OF MAIN FET
10
20
TIME t (nsec)

FIG. 2B

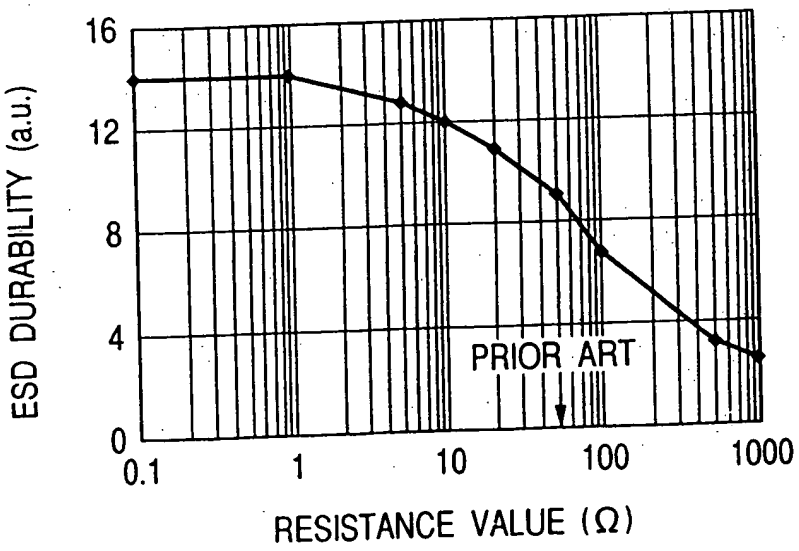

ESD DURABILITY (a.u.)
16
12
8
4
0
0.1
1
10
100
1000
PRIOR ART
RESISTANCE VALUE (Ω)

FIG. 3

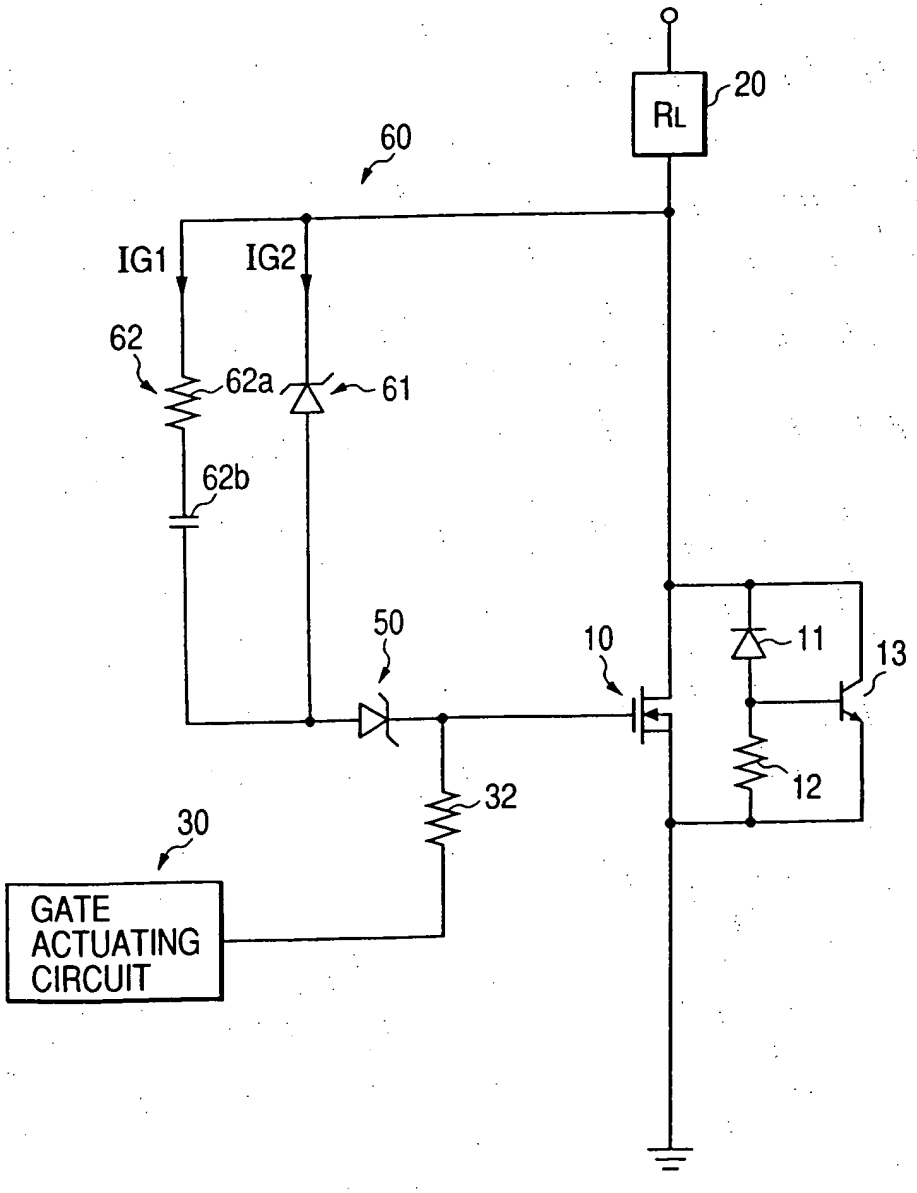

RL
20
60
IG1
IG2
62
62a
61
62b
50
10
11
13
12
32
30
GATE
ACTUATING
CIRCUIT

FIG. 4

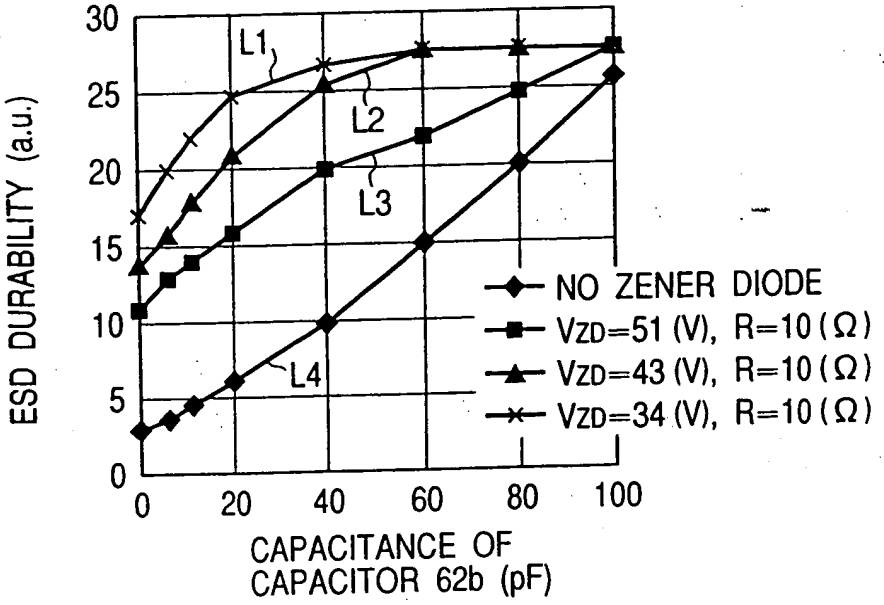

ESD DURABILITY (a.u.)
30
25
20
15
10
5
0
0
20
40
60
80
100
CAPACITANCE OF CAPACITOR 62b (pF)
L1
L2
L3
L4
NO ZENER DIODE
VZD=51 (V), R=10 (Ω)
VZD=43 (V), R=10 (Ω)
VZD=34 (V), R=10 (Ω)

FIG. 5

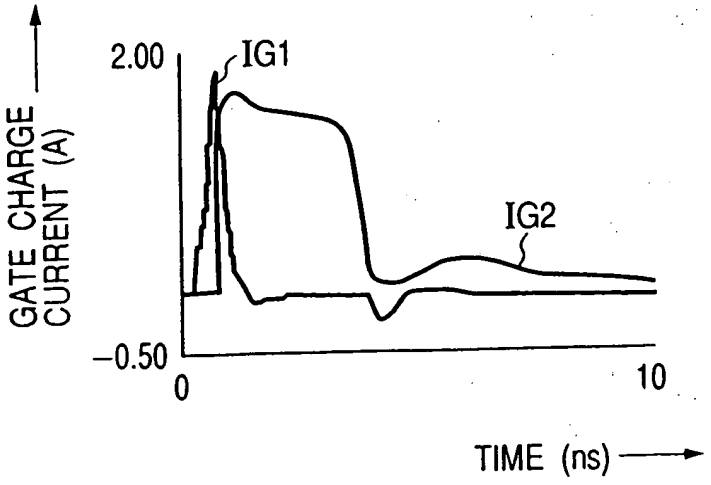

GATE CHARGE CURRENT (A)
2.00
−0.50
0
10
IG1
IG2
TIME (ns)

FIG. 6

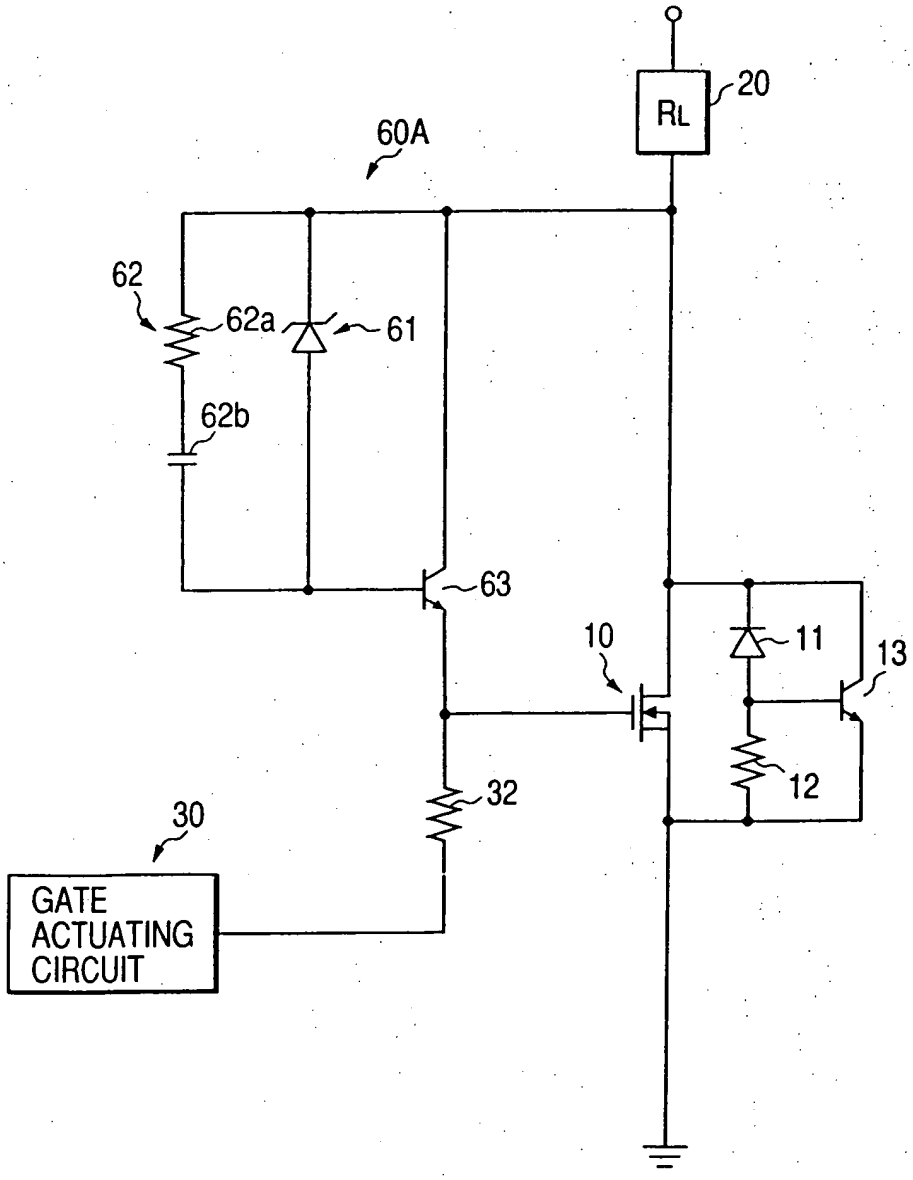

RL
20
60A
62
62a
61
62b
63
10
11
13
12
32
30
GATE
ACTUATING
CIRCUIT

FIG. 7

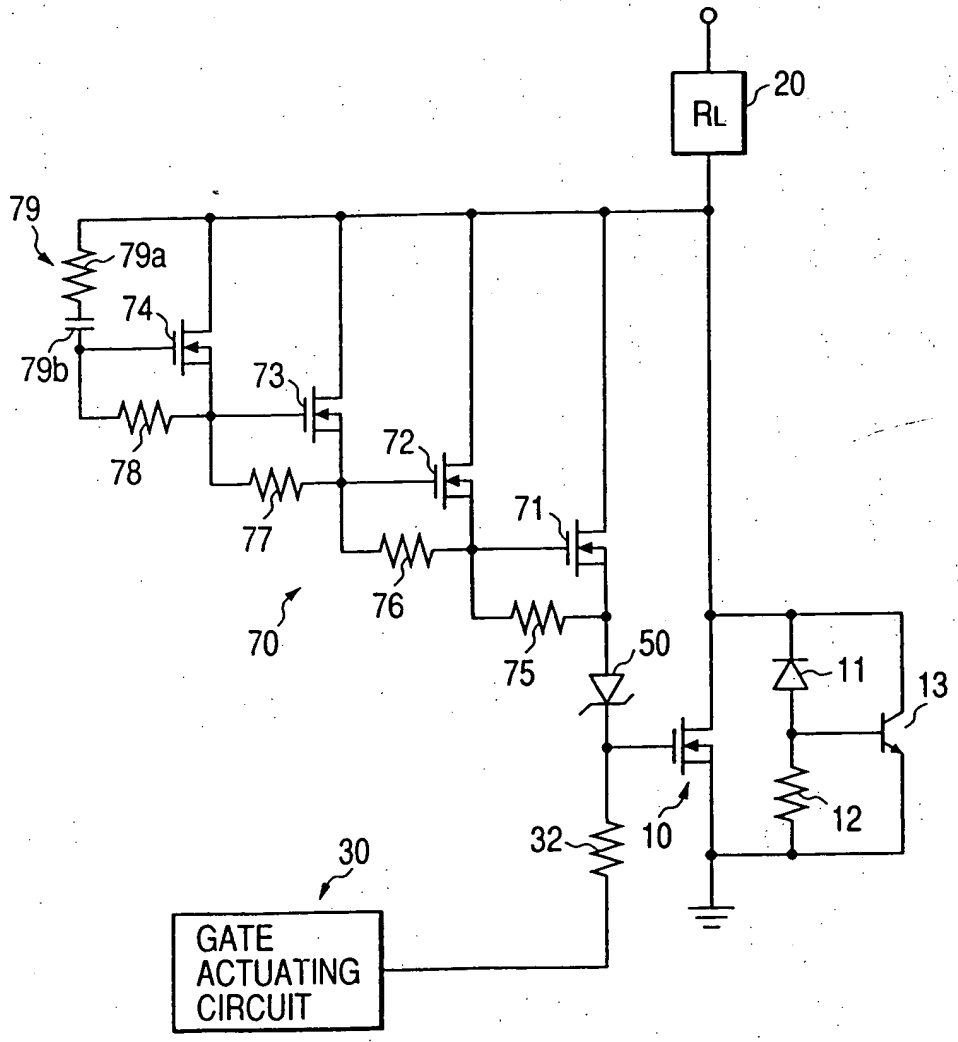

RL
20
79
79a
74
79b
73
78
72
77
71
76
70
75
50
11
13
12
10
32
30
GATE
ACTUATING
CIRCUIT

FIG. 8

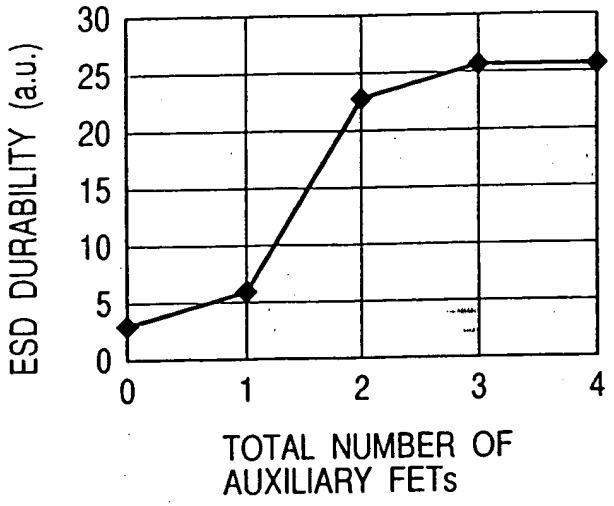


FIG. 10

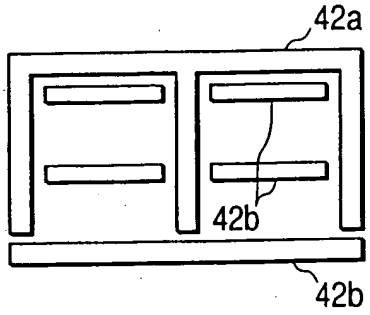


FIG. 11 PRIOR ART

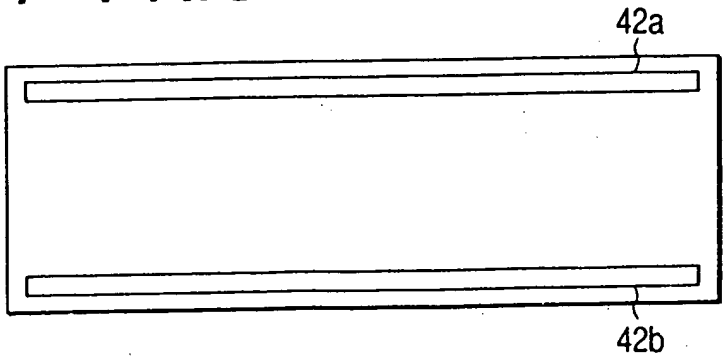


FIG. 9

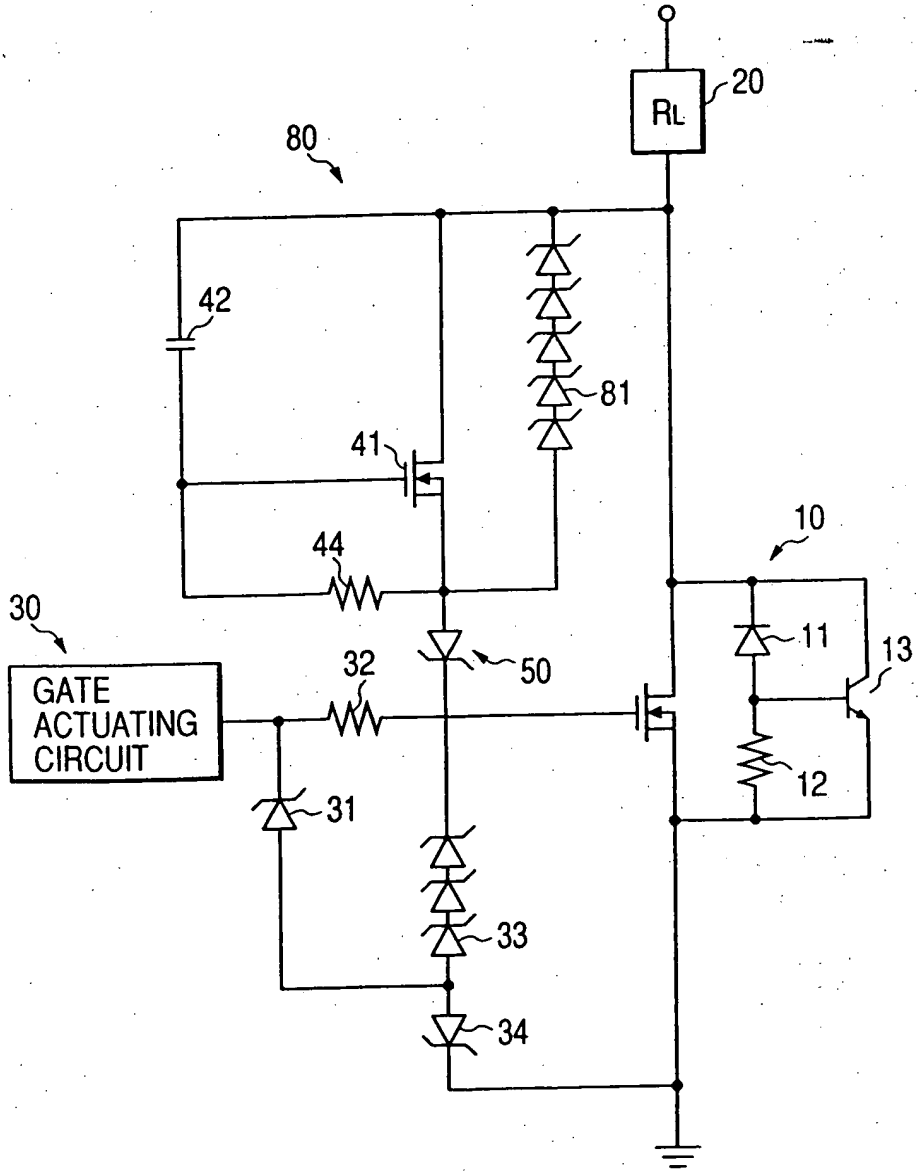

RL
20
80
42
81
41
44
10
30
GATE
ACTUATING
CIRCUIT
32
50
11
13
12
31
33
34

FIG. 12A

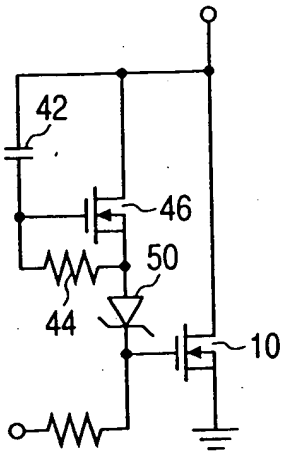


FIG. 12B

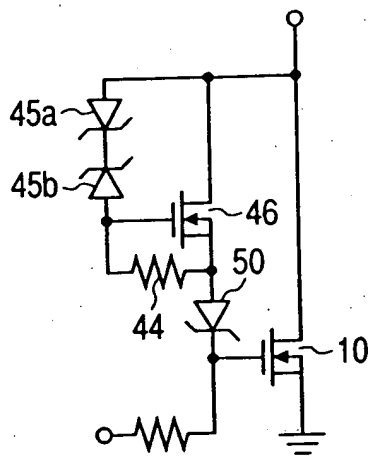


FIG. 14

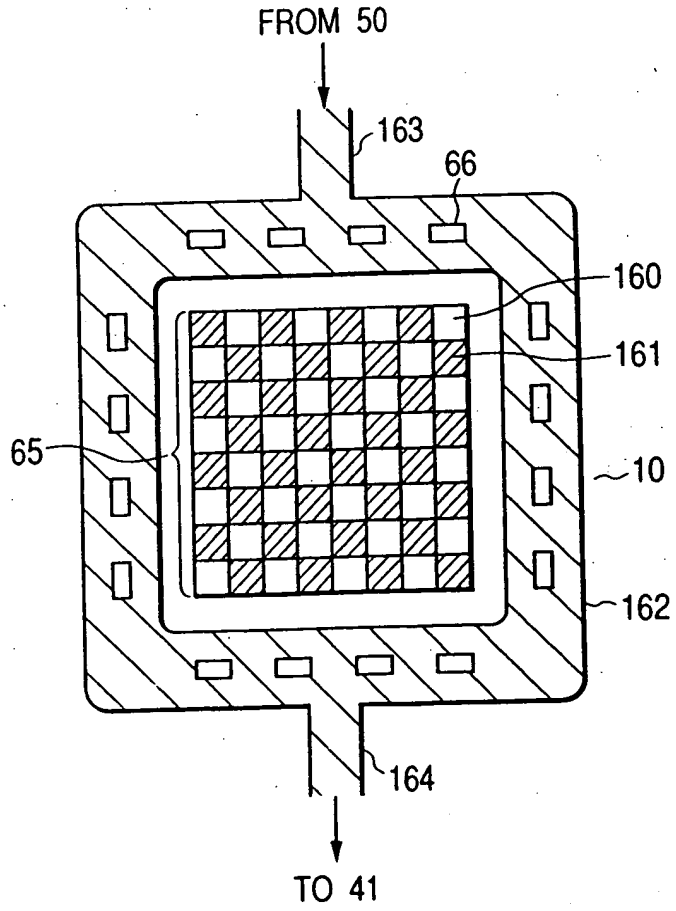


FIG. 13A

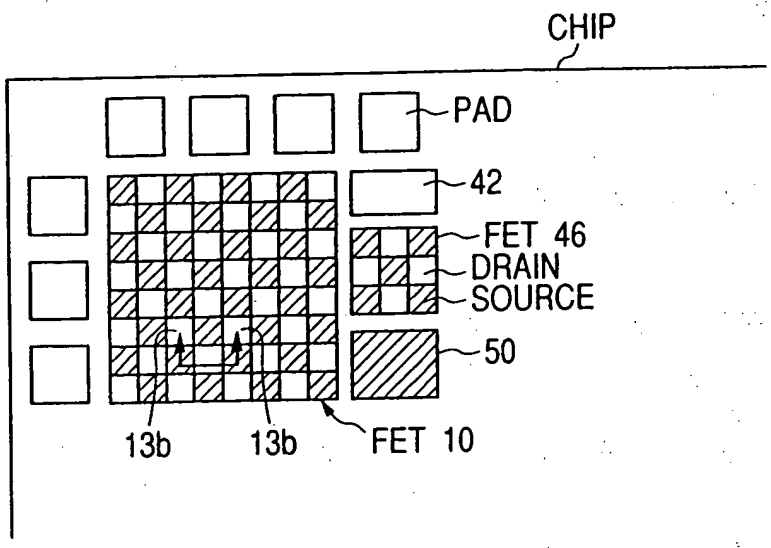


FIG. 13B

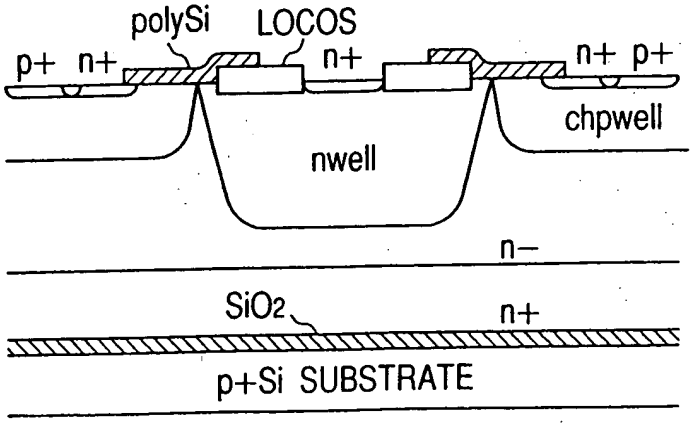


FIG. 15A

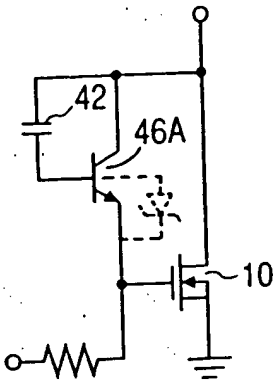


FIG. 15B

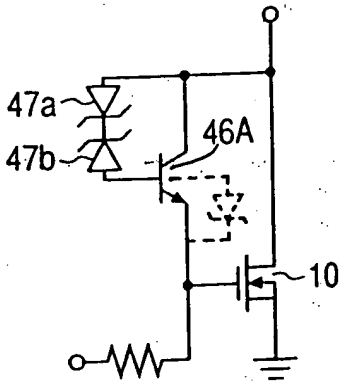


FIG. 16A

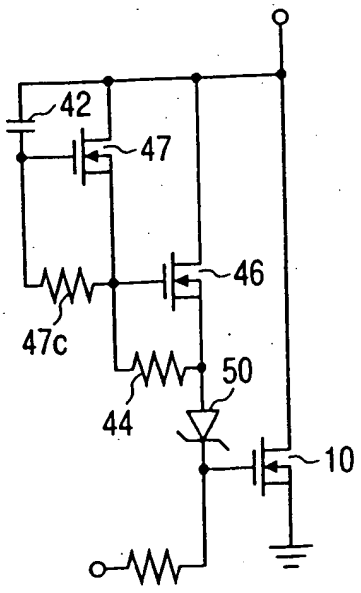


FIG. 16B

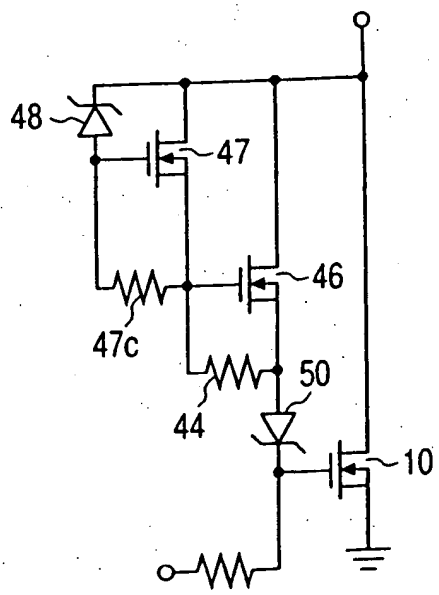


FIG. 17A

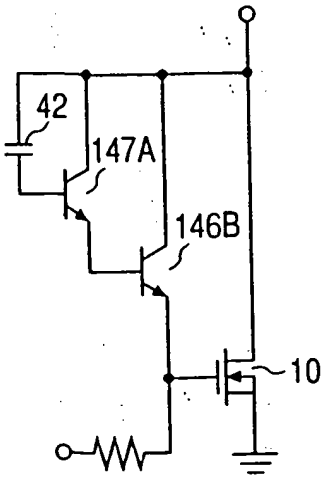


FIG. 17B

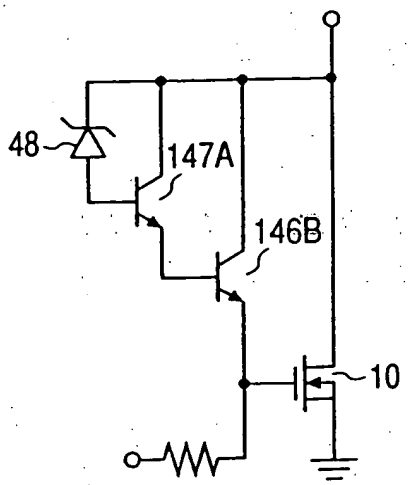


FIG. 18A

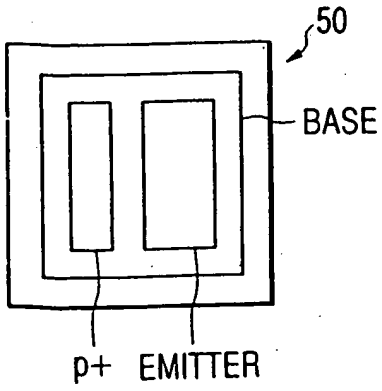


FIG. 18B
PRIOR ART

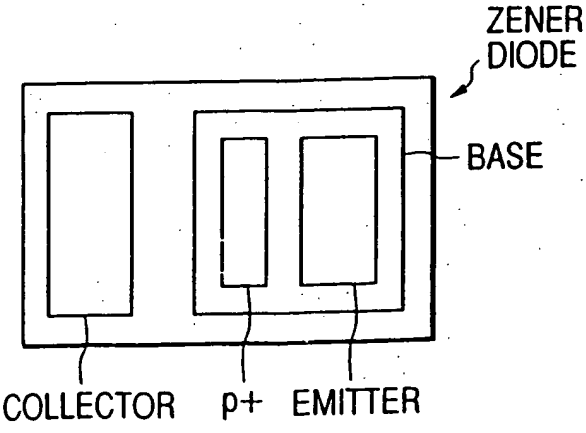


FIG. 19

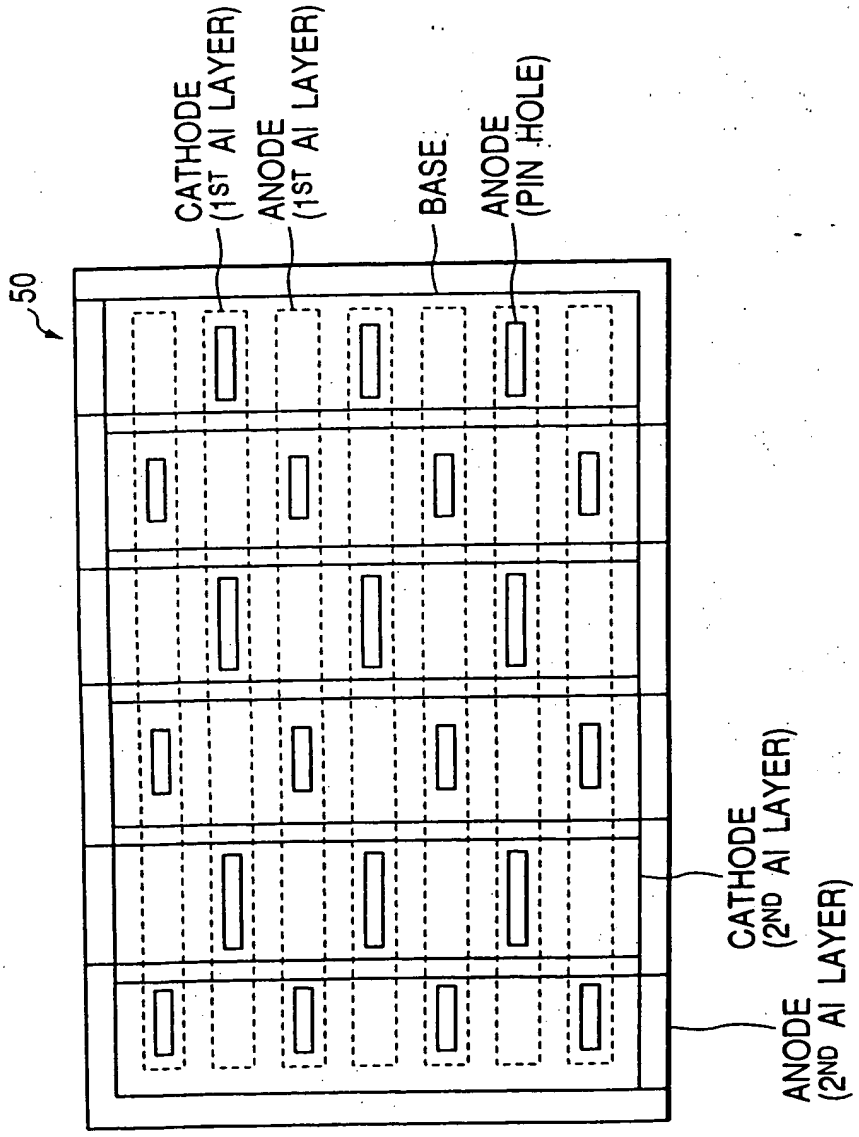

50
CATHODE (1ST Al LAYER)
ANODE (1ST Al LAYER)
BASE
ANODE (PIN HOLE)
CATHODE (2ND Al LAYER)
ANODE (2ND Al LAYER)

FIG. 20A

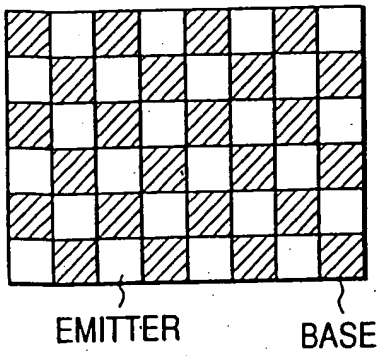


FIG. 20B

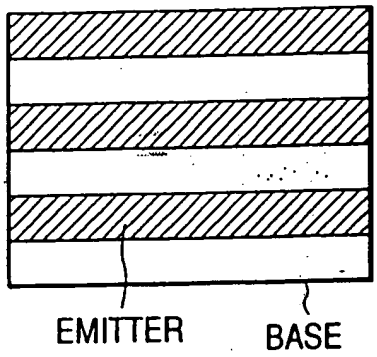


FIG. 21

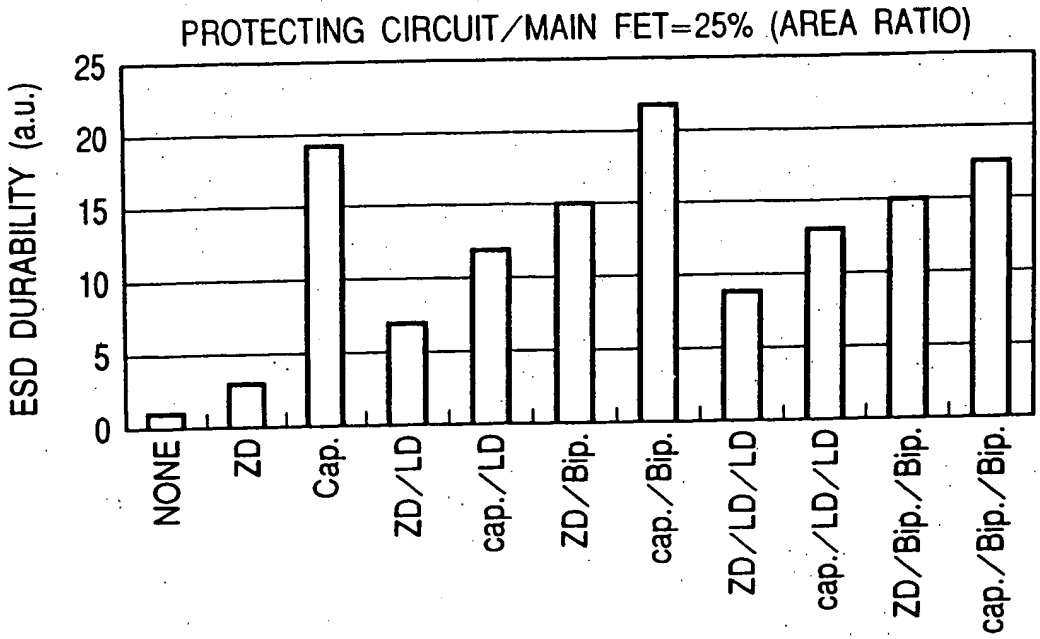


FIG. 22 PRIOR ART

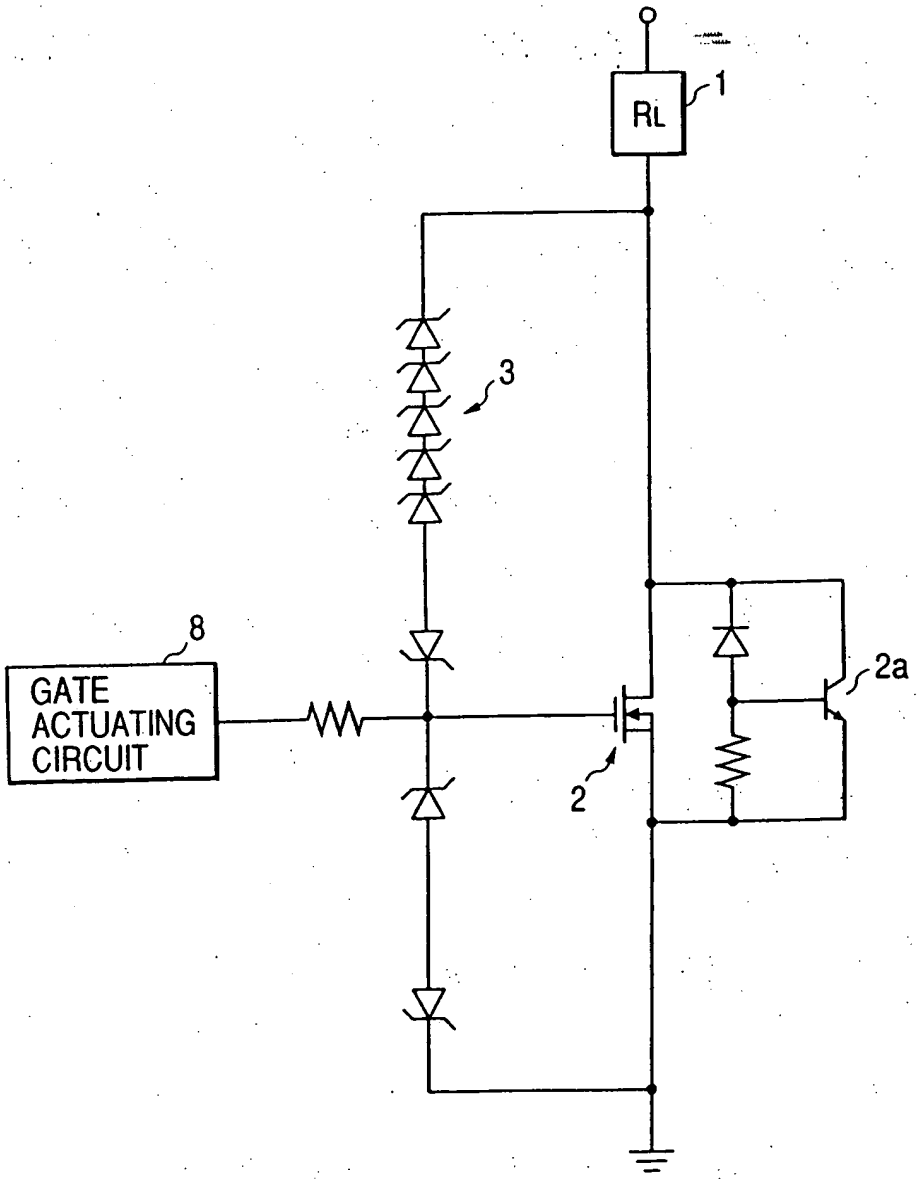


FIG. 23 PRIOR ART

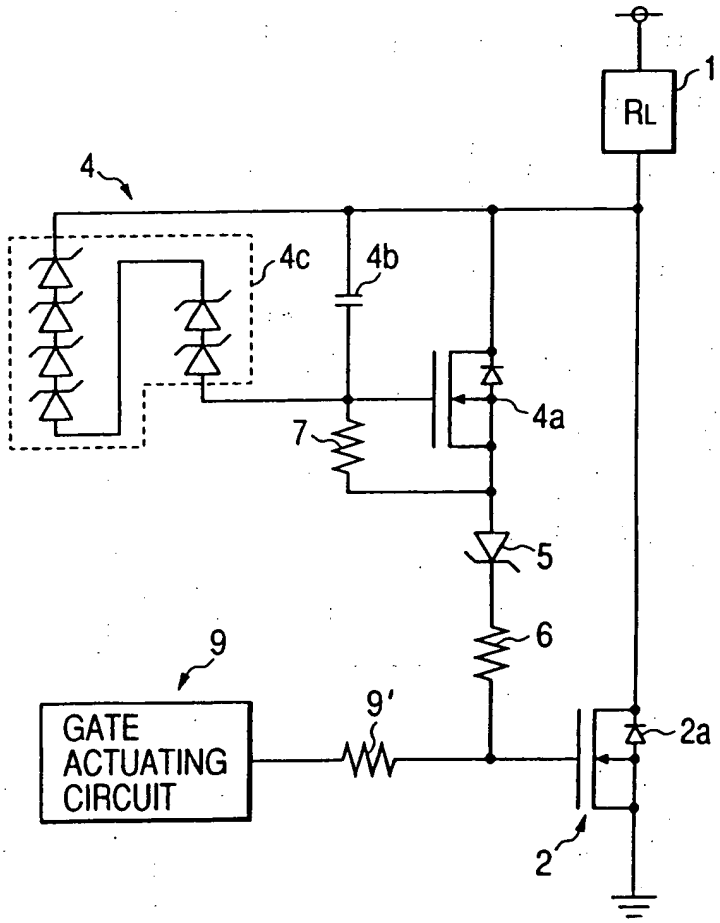


FIG. 24

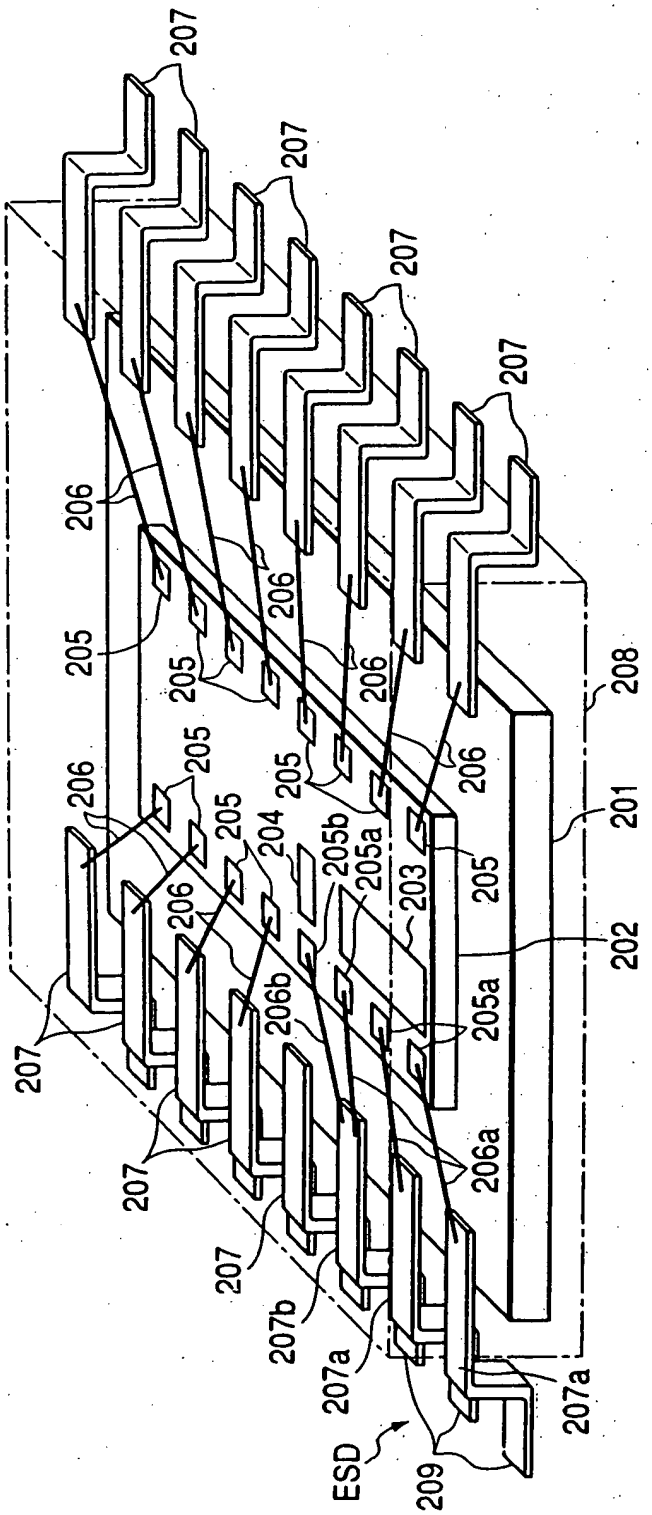

207
207
207
207
206
206
205
205
206
205
205
206
205
206
208
205
204
205b
205a
203
205
201
206
206b
202
205a
207
206a
207
207b
207a
207a
ESD
209

FIG. 25

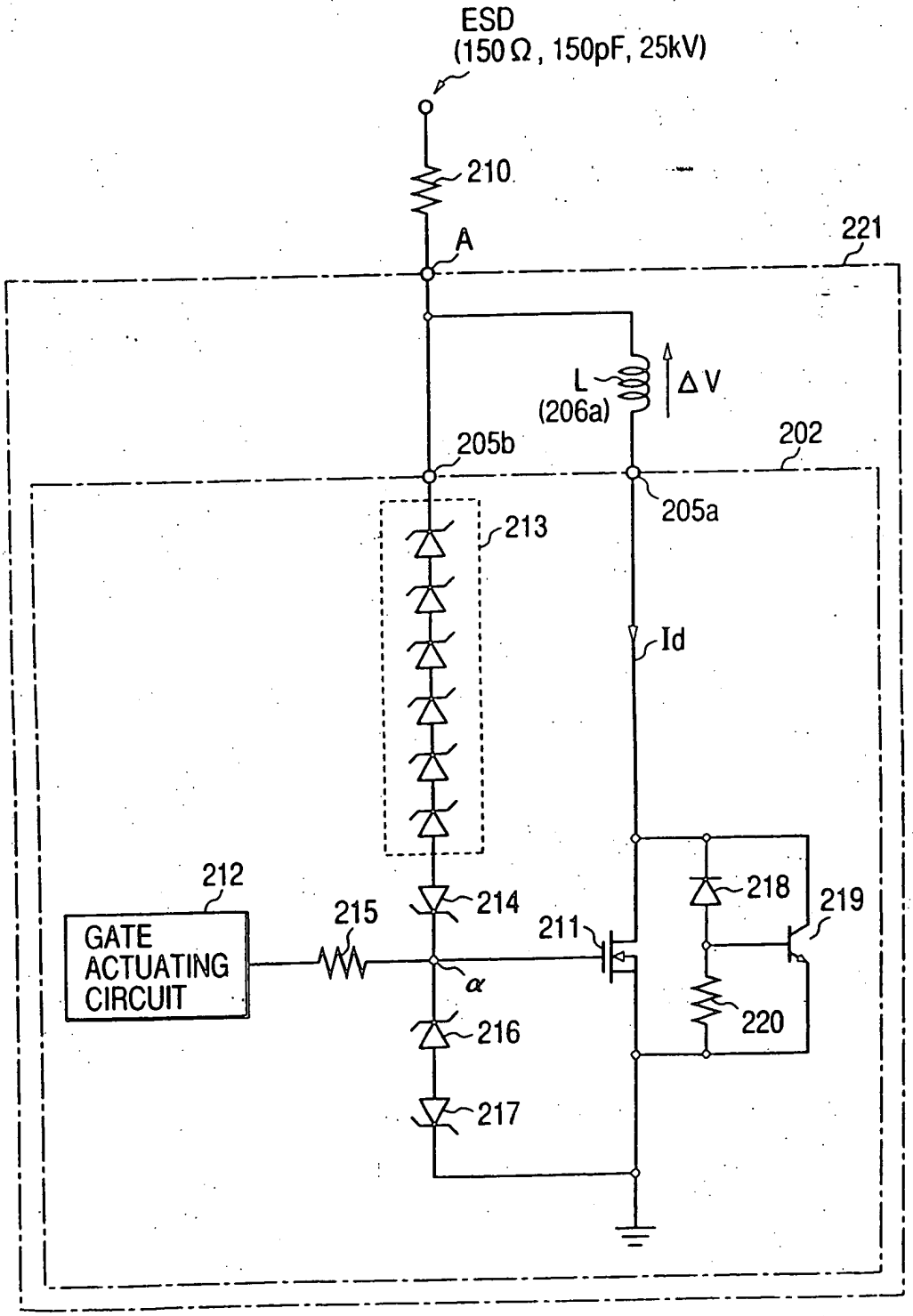

ESD
(150 Ω, 150pF, 25kV)
210
A
221
L
(206a)
ΔV
205b
202
205a
213
Id
212
GATE
ACTUATING
CIRCUIT
215
214
211
218
219
α
220
216
217

FIG. 26

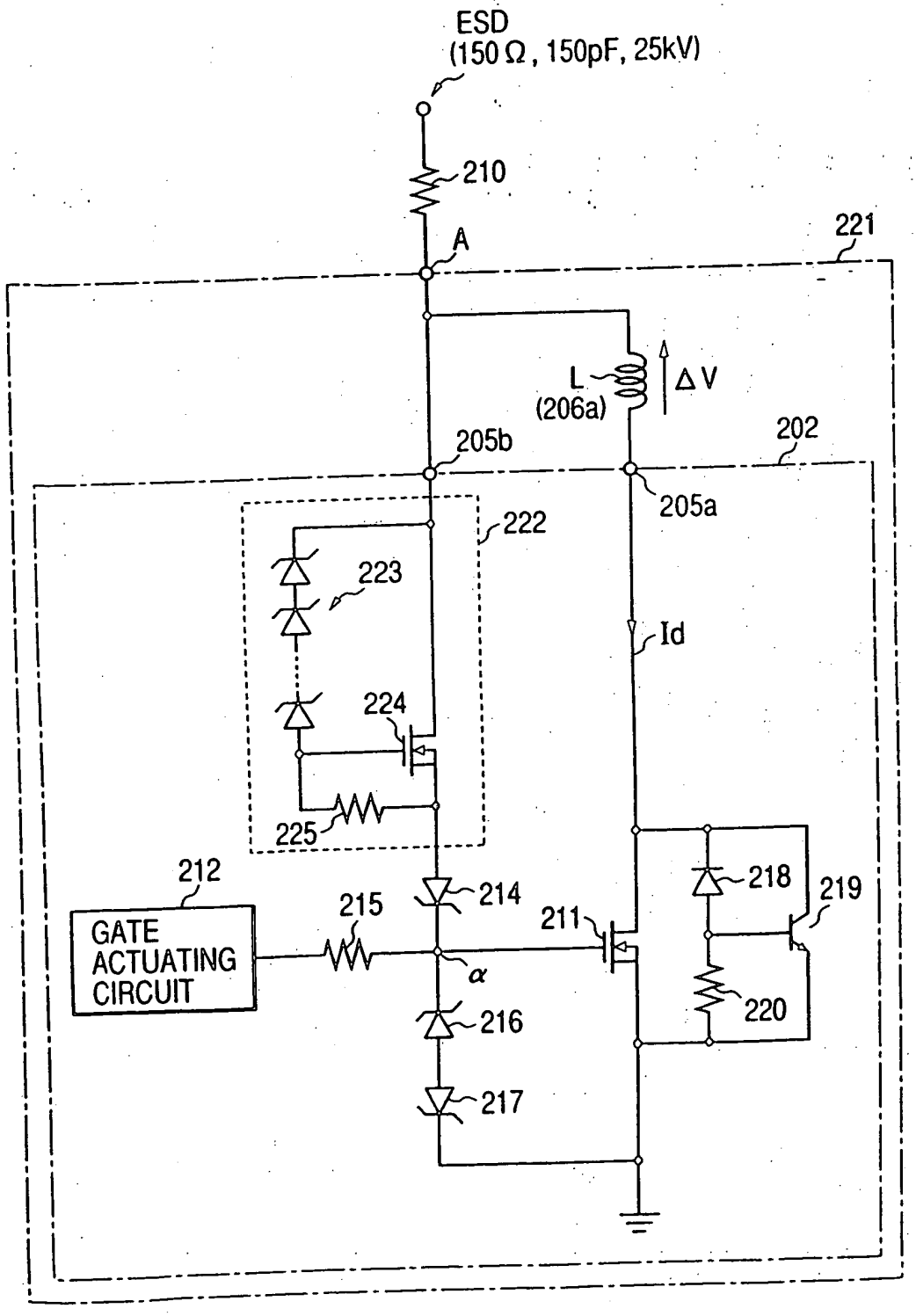

ESD
(150 Ω, 150pF, 25kV)
210
A
221
L
(206a)
ΔV
205b
202
205a
222
223
Id
224
225
212
GATE
ACTUATING
CIRCUIT
215
214
211
218
219
α
220
216
217

FIG. 27

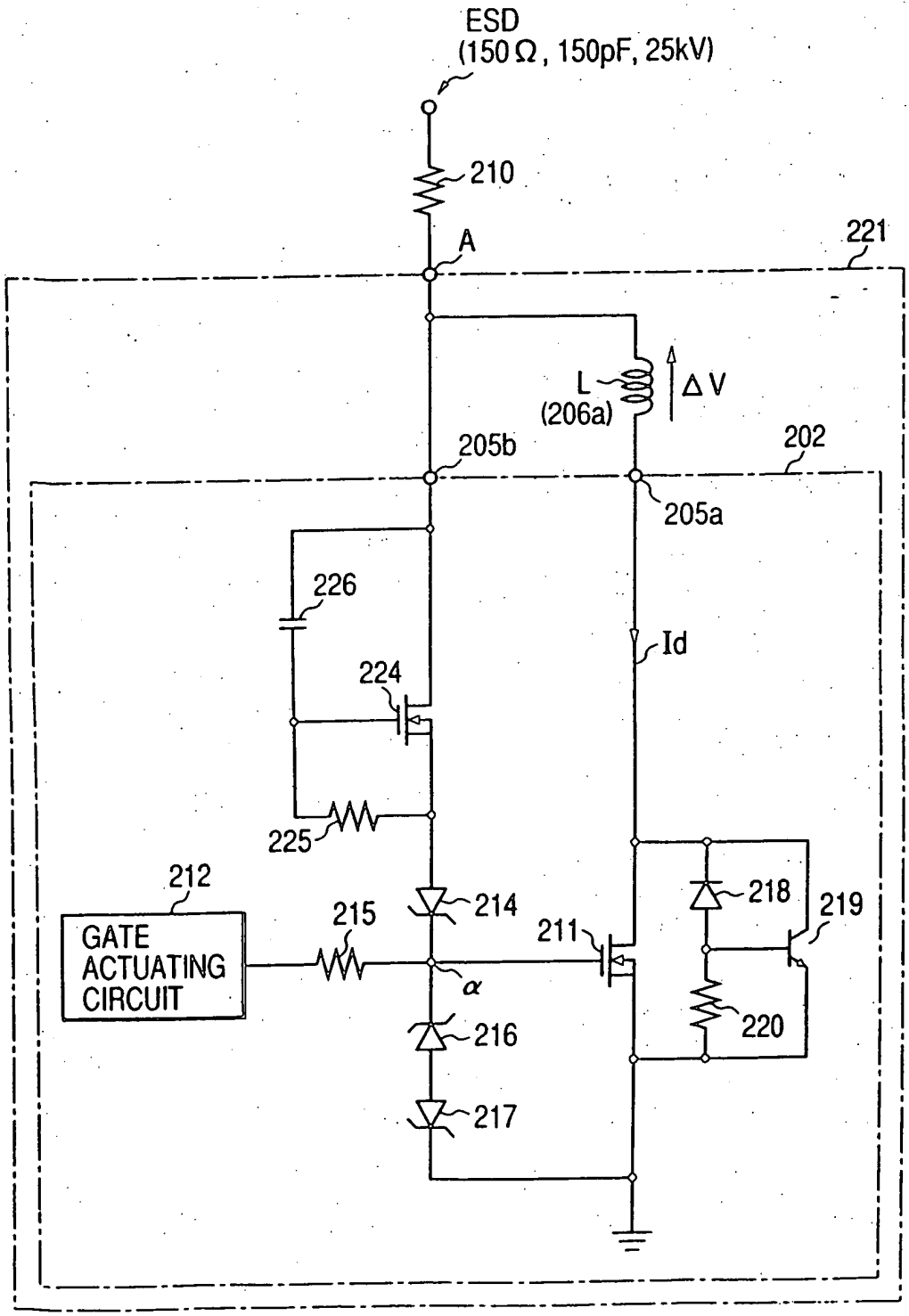

ESD
(150Ω, 150pF, 25kV)
210
A
221
L
(206a)
ΔV
205b
202
205a
226
Id
224
225
212
GATE
ACTUATING
CIRCUIT
215
214
211
218
219
α
220
216
217

FIG. 28

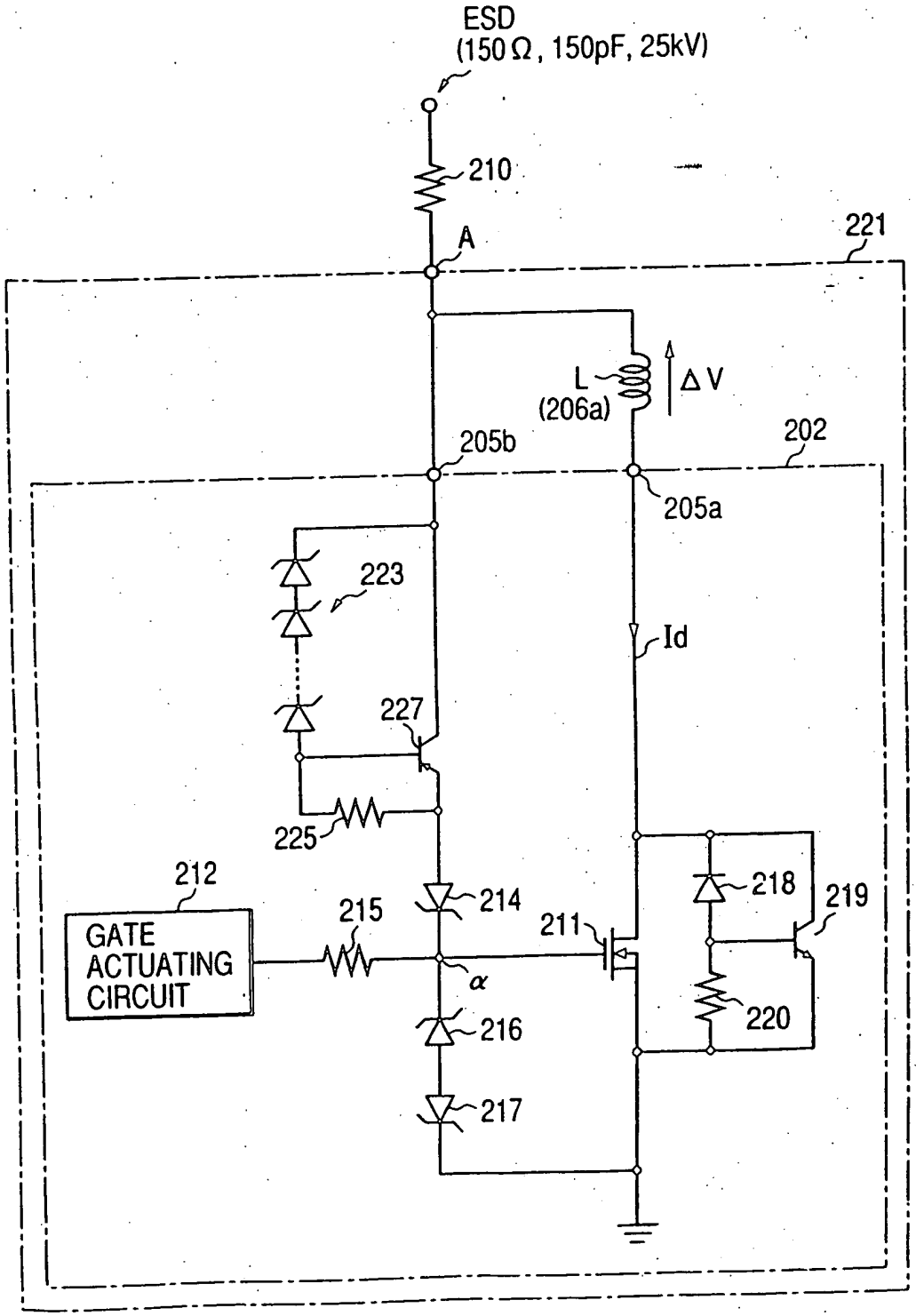

ESD
(150Ω, 150pF, 25kV)
210
A
221
L
(206a)
ΔV
205b
202
205a
223
Id
227
225
212
GATE
ACTUATING
CIRCUIT
215
214
211
218
219
α
220
216
217

FIG. 29

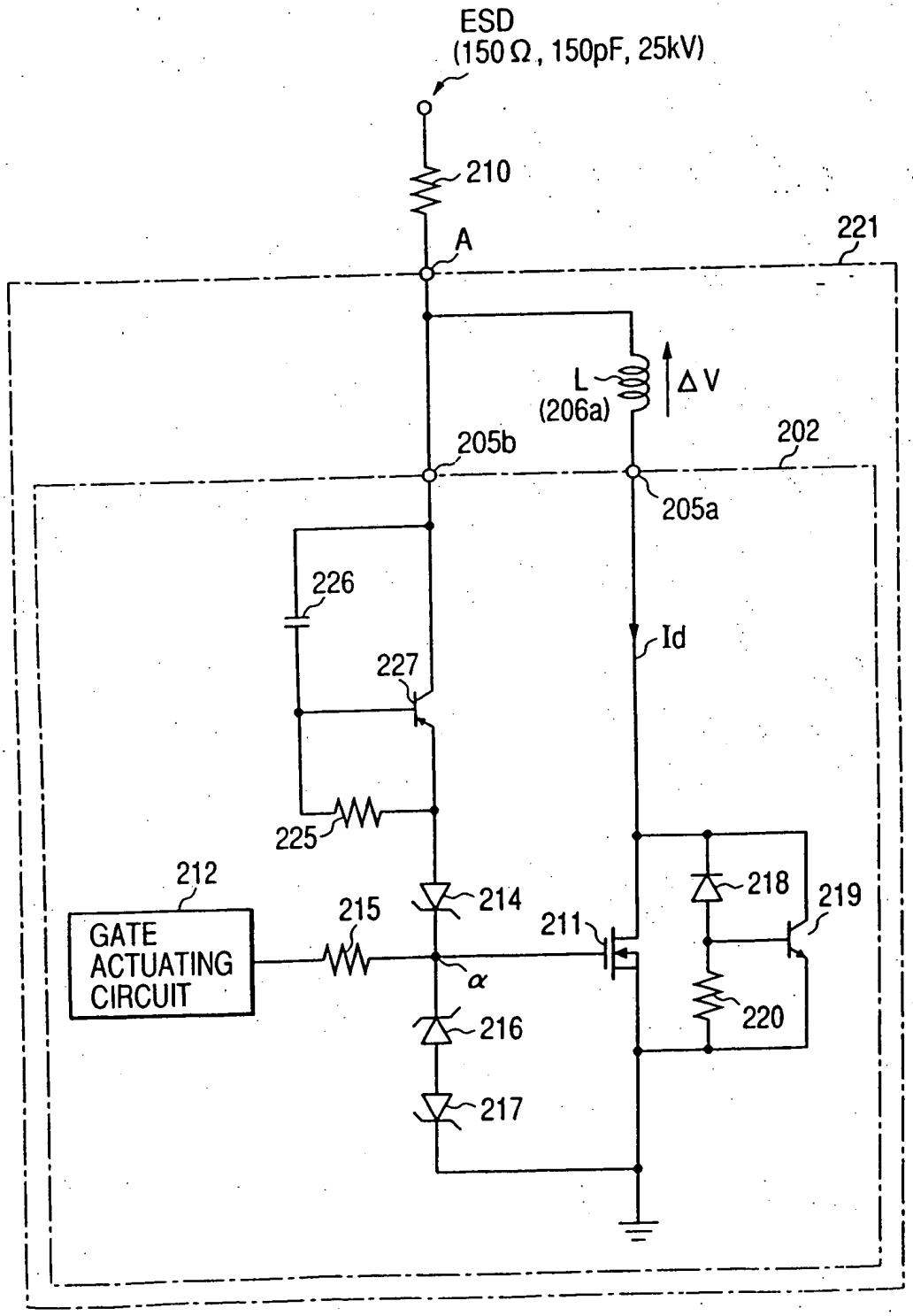

ESD
(150 Ω, 150pF, 25kV)
210
A
221
L
(206a)
ΔV
205b
202
205a
226
Id
227
225
212
GATE
ACTUATING
CIRCUIT
215
214
211
218
219
α
220
216
217

FIG. 30

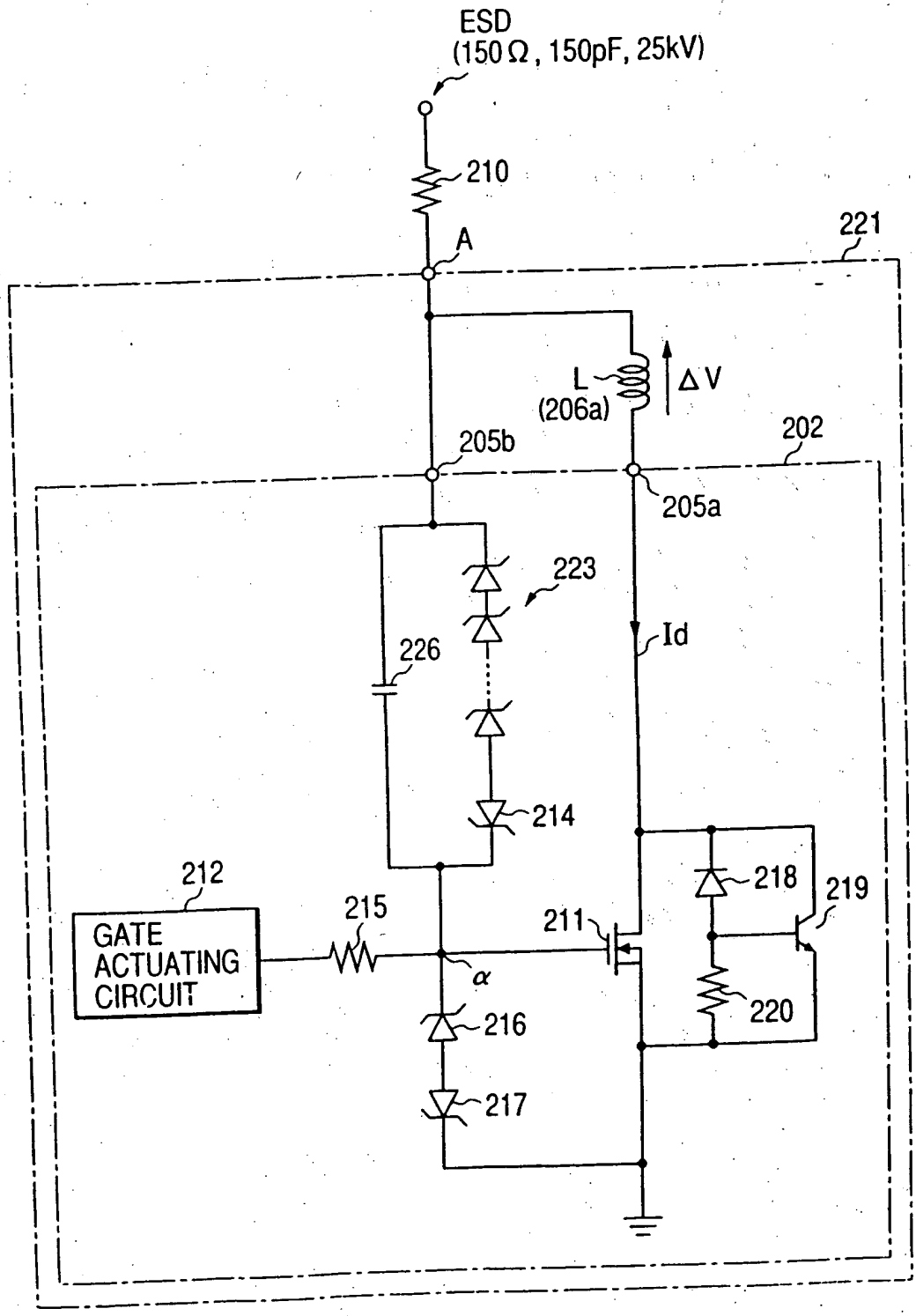
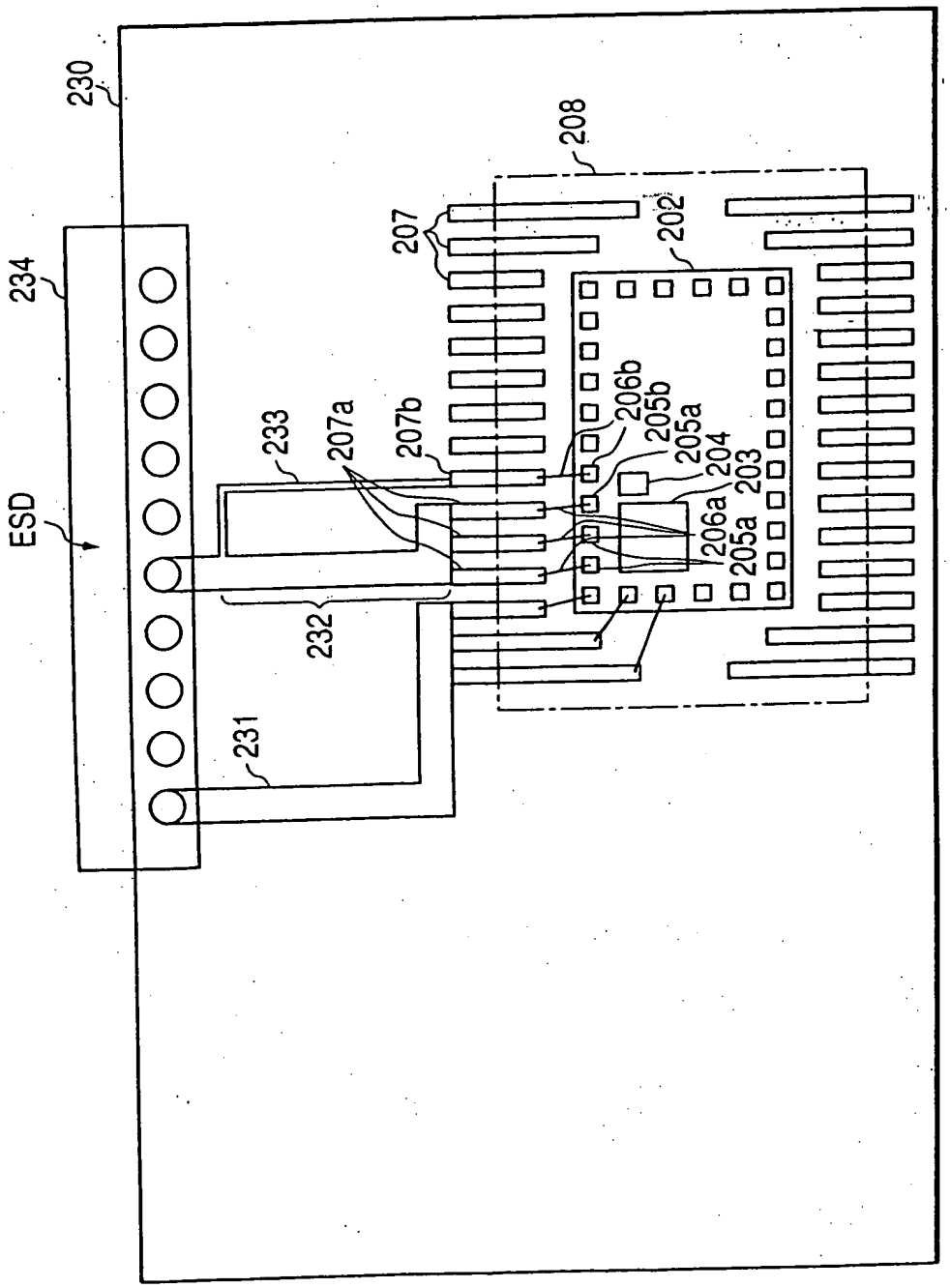

ESD
(150Ω, 150pF, 25kV)
210
A
221
L
(206a)
ΔV
205b
202
205a
223
226
Id
214
212
GATE
ACTUATING
CIRCUIT
215
211
218
219
α
220
216
217

FIG. 31


230
208
207
202
234
233
207a
207b
206b
205b
205a
204
203
206a
205a
ESD
232
231

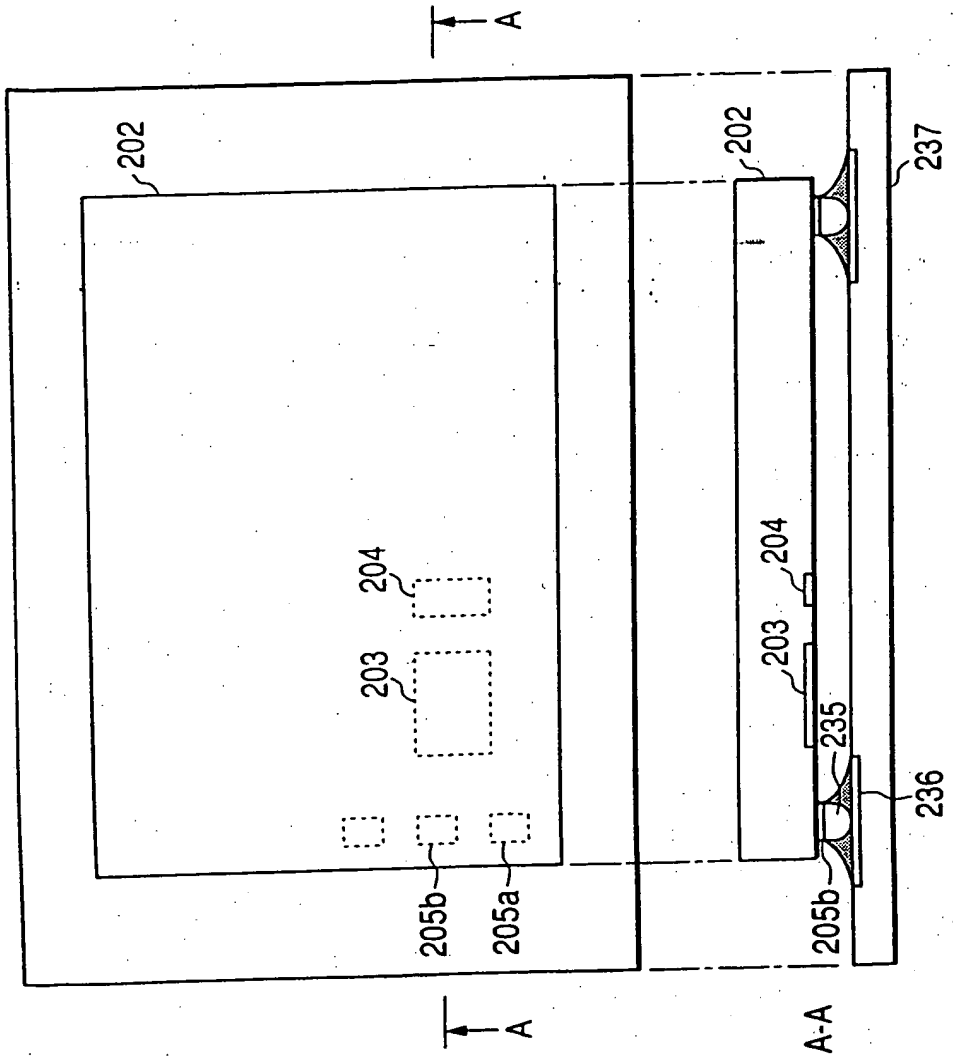


FIG. 32A

FIG. 32B

FIG. 33

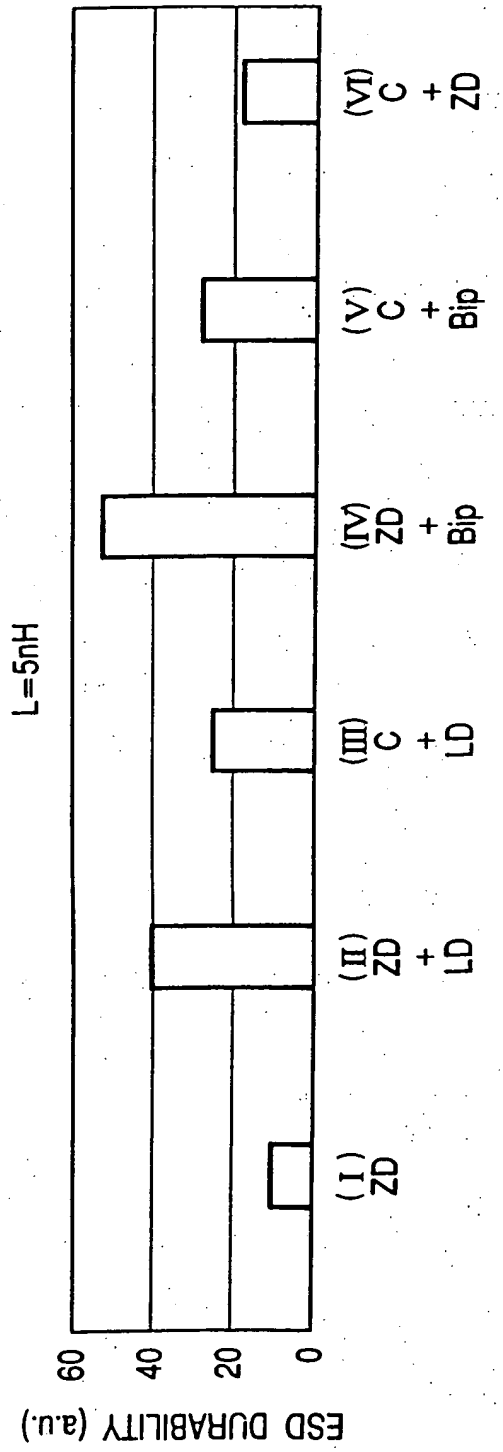

L=5nH
ESD DURABILITY (a.u.)
60
40
20
0
(I) ZD
(II) ZD + LD
(III) C + LD
(IV) ZD + Bip
(V) C + Bip
(VI) C + ZD

FIG. 34

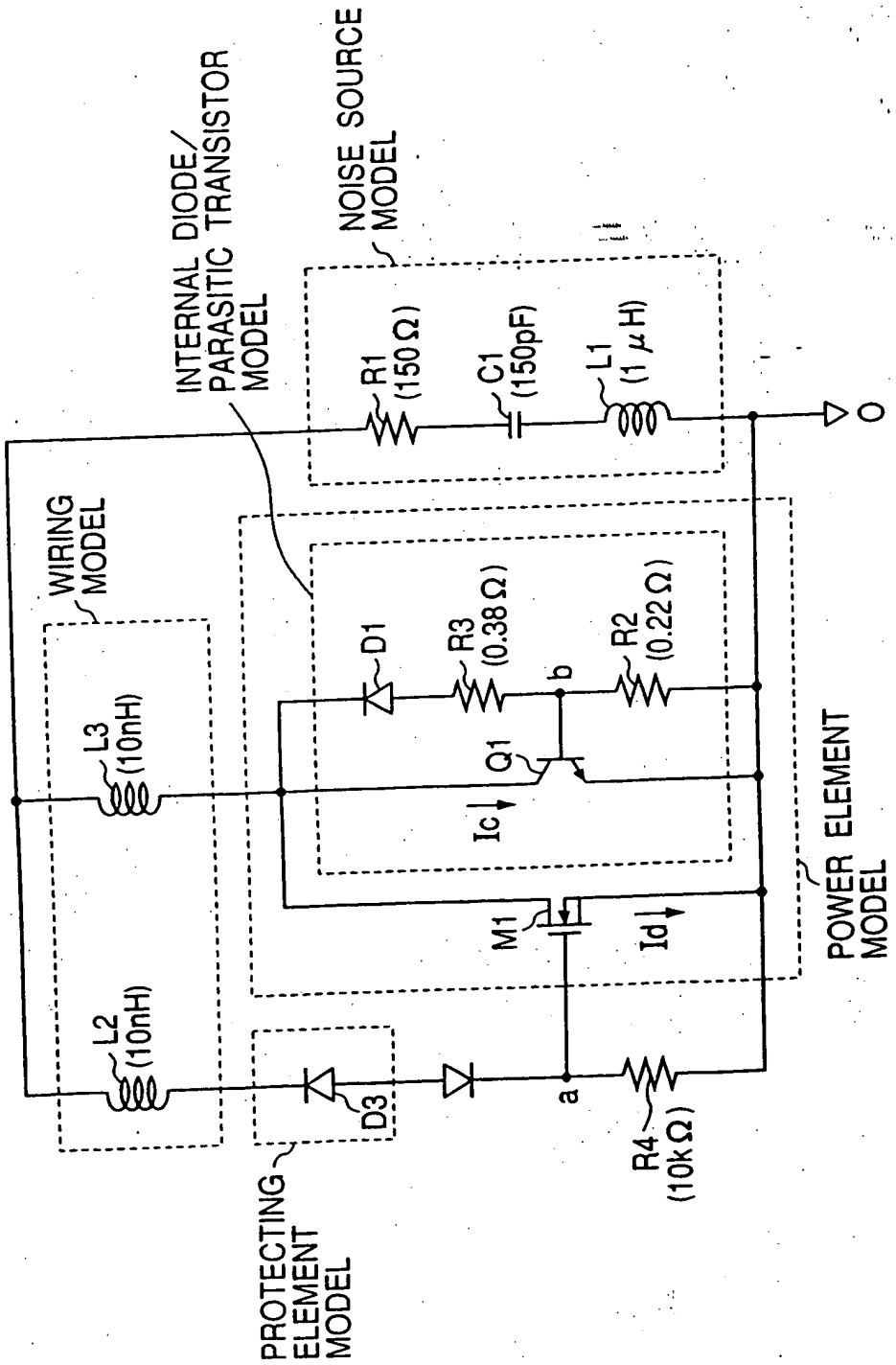

INTERNAL DIODE/
PARASITIC TRANSISTOR
MODEL
NOISE SOURCE
MODEL
R1
(150 Ω)
C1
(150pF)
L1
(1 μH)
O
WIRING
MODEL
L3
(10nH)
D1
R3
(0.38 Ω)
b
R2
(0.22 Ω)
Q1
Ic
M1
Id
POWER ELEMENT
MODEL
L2
(10nH)
D3
a
R4
(10kΩ)
PROTECTING
ELEMENT
MODEL

FIG. 35

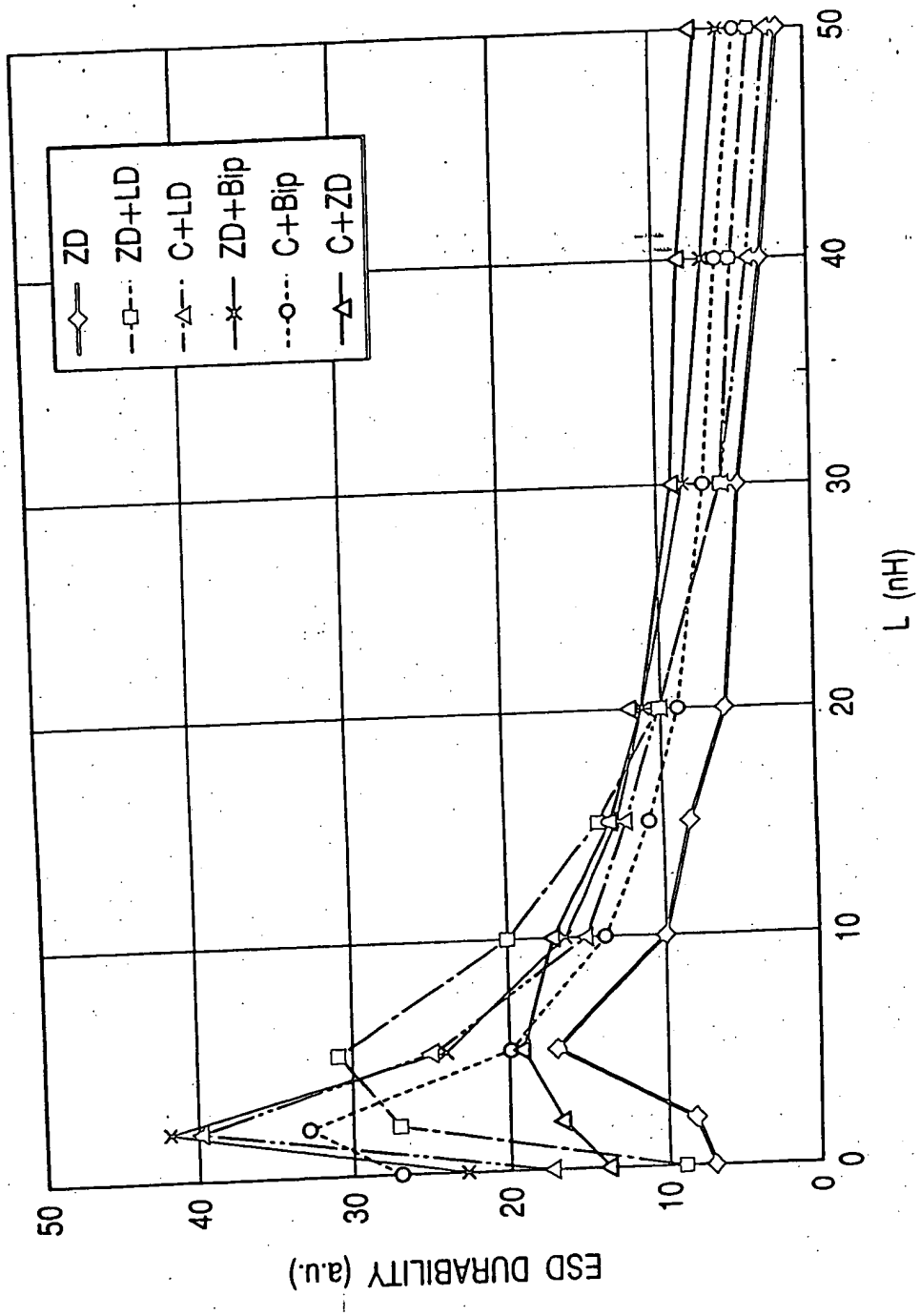

ZD
ZD+LD
C+LD
ZD+Bip
C+Bip
C+ZD
ESD DURABILITY (a.u.)
L (nH)
0
10
20
30
40
50

FIG. 36A

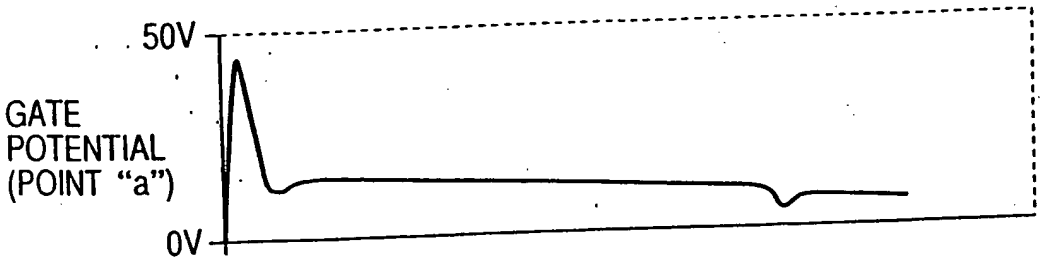


FIG. 36B

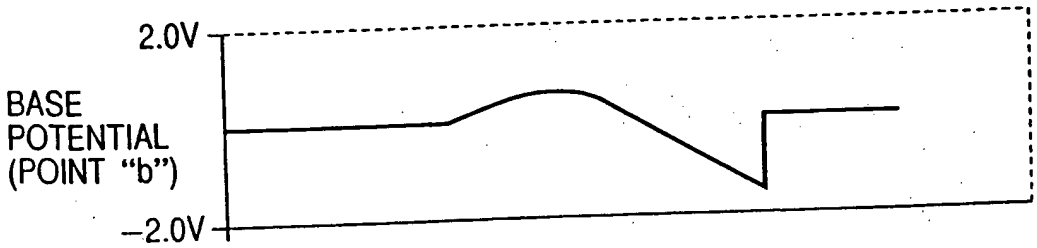


FIG. 36C

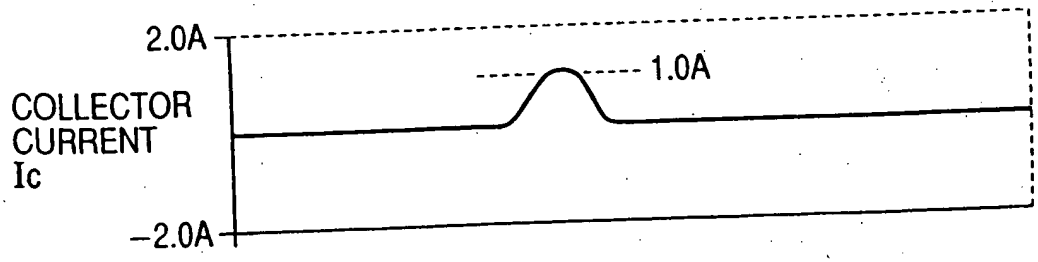


FIG. 36D